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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/830,188
Filing Date: April 21, 2004
Appellant(s): LANE ET AL.

William Marcus Hooks
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 17 November 2008 appealing from the Office action mailed 3 November 2005.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 5,468,999 | Lin et al. | 11-1995 |
| 5,691,568 | Chou et al. | 11-1997 |
| 5,898,213 | Torres et al. | 04-1999 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-12 and 14 are rejected under 35 U.S.C. 103(a). This rejection was set forth in the prior Office Action, mailed 3 November 2005.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Torres et al. (5,898,213) in view of Lin et al. (5,468,999).

Torres et al. disclose a method of making a semiconductor package where a substrate (95) has a die (96) mounted at a die attach area; the die (96) has a plurality of

bond pads (97); bond pad islands (98) are located on the substrate (95); bond wire (99) connects the bond pad (97) to the bond island (98); the bond pad island (98) is connected to a conductive terminal pad (102) by trace (101) (Fig. 7; col. 5, lines 1- 27). Torres et al. further disclose encapsulating the die (col. 6, lines 56-67). Torres et al. also disclose the package lead comprises a solder ball included in a ball grid array (BGA) (col. 1, lines 1-2) or a land included in a land grid array (LGA) (col. 5,lines 40-48). Torres et al. do not disclose connecting a plurality of solder balls to the at least one bond island, wherein at least on redundant solder ball is used to form a path for the inner solder balls connected to bond islands to be electrically plated.

Lin et al. disclose a method of making a semiconductor package where a substrate (14/16) has a die (12) mounted at a die attach area; bond wire (28) connecting the die (12) and the substrate (14/16); a conductive terminal pad (20) (col. 4, line 44 thru col. 5, line 24). Lin et al. further disclose connecting a plurality of solder balls (34), the plurality of solder balls being located inwardly from an edge of the substrate (14/16), wherein at least on redundant solder ball (34) which may be used to form a path for the inner solder balls connected to be electrically plated (col. 4, lines 55-64).

Since Torres et al. and Lin et al. are both from the same field of endeavor, a method of making a semiconductor package, the purpose disclosed by Lin et al. would have been recognized in the pertinent art of Torres et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Torres et al. by connecting a plurality of solder balls, the plurality of solder balls being

located inwardly from an edge of the substrate, wherein at least on redundant solder ball is used to form a path for the inner solder balls connected to be electrically plated as taught by Lin et al. to increase the number of input/output terminals without causing electrical shorts and without increasing the size of the package (col. 1, line 57 thru col. 2, line 6).

Claims 6-10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Torres et al. in view of Lin et al. as applied to claim 1 above, and further in view of Chou et al. (5,691,568).

Torres et al. in view of Lin et al. disclose the subject matter claimed above except a bond finger for coupling a bond wire between a bond finger and a bond pad.

Chou et al. disclose a method of making a semiconductor package where a package comprises a bond finger (511) for coupling a bond wire (526b) between a bond finger and a bond pad on the semiconductor chip (Fig. 5b; col. 10, lines 4-58; col. 12, lines 4-30).

Since Torres et al. and Chou et al. are both from the same field of endeavor, a method of making a semiconductor package, the purpose disclosed by Chou et al. would have been recognized in the pertinent art of Torres et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Torres et al. by forming a bond finger for coupling a bond wire between a bond finger and a bond pad as taught by Chou et al. to minimize false switching (col. 5, lines 22-45).

**(10) Response to Argument**

The appellant argues three points: (1) there is no motivation to combine the Torres et al. and Lin et al. references; (2) Lin et al. does not disclose the claimed connecting of the solders balls and using at least one redundant solder ball to form a path for the inner solder balls connected to bond islands to be electrically plated; and (3) the combination of Torres et al. and Lin et al. do not disclose the claim limitation using at least one redundant solder ball to form a path for the inner solder balls connected to bond islands to be electrically plated.

In response to appellant's first argument, there is proper motivation to combine the Torres et al. and Lin et al. references. Torres et al. disclose a method of making a semiconductor package where a substrate has a die mounted at a die attach area; the die has a plurality of bond pads; bond pad islands are located on the substrate; bond wire connects the bond pad to the bond island; the bond pad island is connected to a conductive terminal pad by trace (Fig. 7; col. 5, lines 1- 27). However, Torres et al. do not disclose connecting a plurality of solder balls to the at least one bond island, wherein at least on redundant solder ball is used to form a path for the inner solder balls connected to bond islands to be electrically plated. Lin et al. discloses connecting a plurality of solder balls, the plurality of solder balls being located inwardly from an edge of the substrate, wherein at least on redundant solder ball which may be used to form a path for the inner solder balls connected to be electrically plated (col. 4, lines 55-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Torres et al. by connecting a plurality of solder balls, the plurality of

solder balls being located inwardly from an edge of the substrate, wherein at least on redundant solder ball which may be used to form a path for the inner solder balls connected to be electrically plated as taught by Lin et al. to increase the number of input/output terminals without causing electrical shorts and without increasing the size of the package (col. 1, line 57 thru col. 2, line 6). Additionally, the redundant solder solder ball in Lin et al. allow high terminal or pin count devices to have smaller footprints (col. 5, lines 1 & 2).

In response to appellant's second and third arguments, Lin et al. does disclose connecting of the solders balls and using at least one redundant solder ball to form a path for the inner solder balls connected to bond islands to be electrically plated, therefore the combination of Torres et al. and Lin et al. do disclose the claim limitations of independent claims 1 and 12. Lin et al. disclose a method of making a semiconductor package where a substrate has a die mounted at a die attach area; bond wire connecting the die and the substrate; a conductive terminal pad (col. 4, line 44 thru col. 5, line 24). Lin et al. further disclose connecting a plurality of solder balls, the plurality of solder balls being located inwardly from an edge of the substrate, wherein at least on redundant solder ball which may be used to form a path for the inner solder balls connected to be electrically plated (Fig. 4; col. 4, lines 55-64). It is irrelevant that each solder ball has a terminal pad, the Lin et al. is used to teach the additional or redundant solder ball. There is no positive recitation of a path for inner solder balls to be electrically plated in independent claims 1 and 12. Therefore due to the placement of the additional or redundant solder balls in Lin et al., the solder balls are capable of

providing a path for inner solder balls to be electrically plated. Because of this, Torres et al. in view of Lin et al. disclose every limitation of independent claims 1 and 12.

These reasons are consistent with the 35 U.S.C. 103(a) rejection made by the examiner beginning on page 2 of the Office Action mailed 3 November 2005. In conclusion, the combinations of references show all of the limitations of the claims and are proper. The examiner submits that the rejections made under 35 U.S.C. 103(a) are proper and should be affirmed.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Pamela Perkins/
PEP
12 February 2009

Conferees:
/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895

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Supervisory Patent Examiner